Sheet: PCR

Power, Clock and Reset
CLK, RESET

File: PCR.sch

Sheet: PRG

Instruction Fetch
PC, ROM, IR, D

File: PRG.sch

Sheet: CU

Control Unit
CU

File: CU.sch

Sheet: RAM

Memory and Adress Unit
MAU, RAM

File: RAM.sch

Sheet: ALU

Arithmetic and Logic Unit
ALU

File: ALU.sch

Sheet: REG

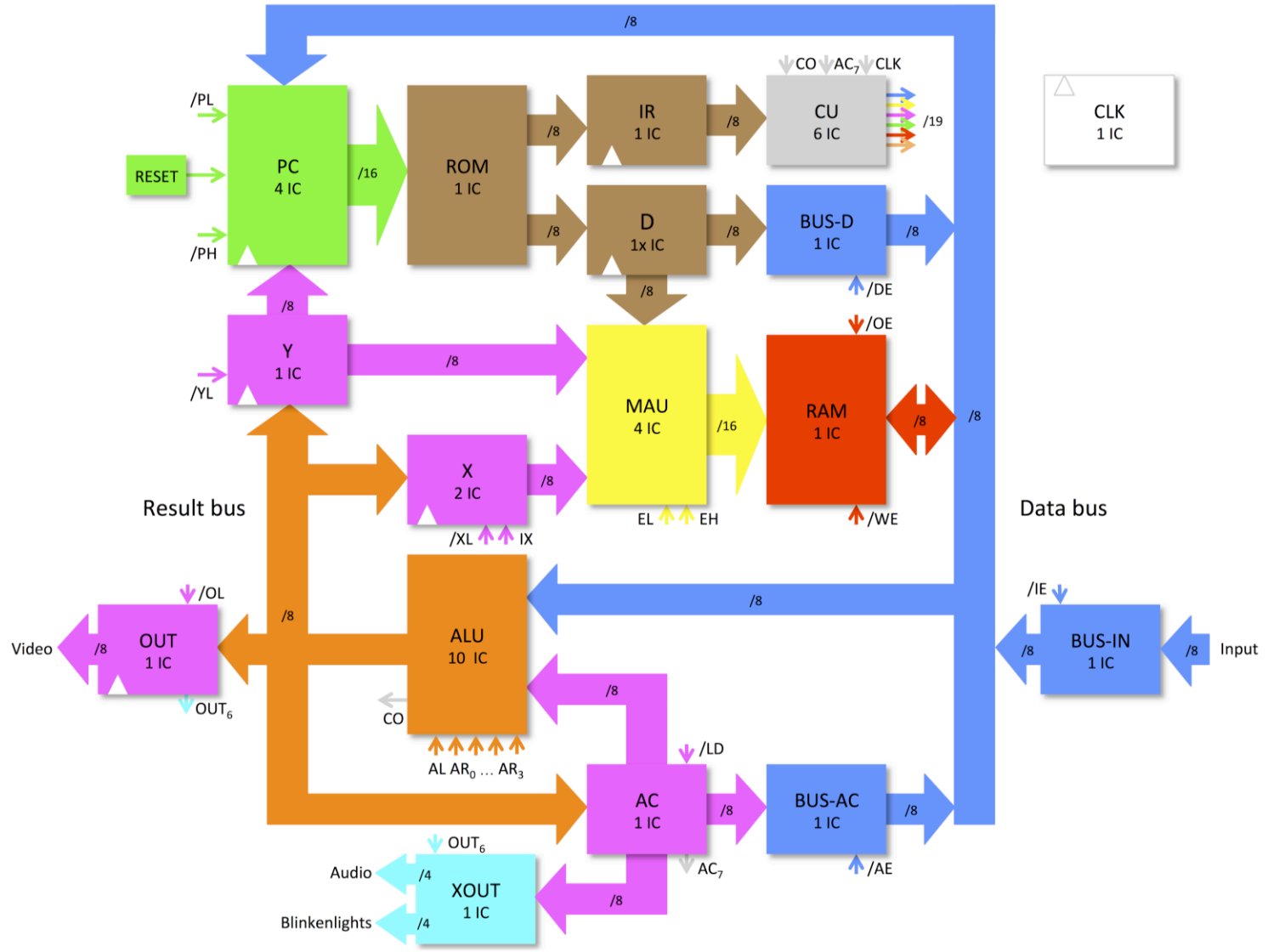
User Registers
AC, X, Y, OUT

File: REG.sch

Sheet: PER

Peripherals
XOUT

File: PER.sch



These schematics use 74HCT but most components can be replaced directly with either 74LS or 74HC. Two notes to keep in mind: (1) 74LS uses more power and has lower V_OH. E.g. when replacing the OUT register with 74LS, adjust the RGB resistors accordingly. (2) For the clock 74HCT always gives the most desirable duty cycle and reliability.

Marcel van Kervinck and Walter Belgers

Sheet: /
File: Gigatron.sch

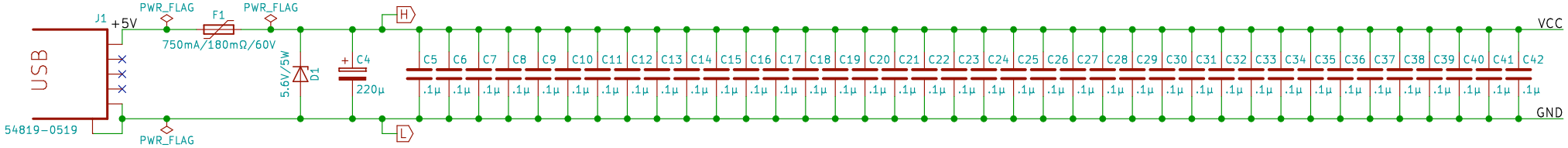
Title: Gigatron TTL microcomputer

Size: A4	Date: 2018-05-10	**Rev: Release**
KiCad E.D.A. kicad 4.0.6		Id: 1/8

Power

Multifuse F1 helps protect the upstream power supply against faults/shorts in the computer (e.g. those caused by build errors or abuse)

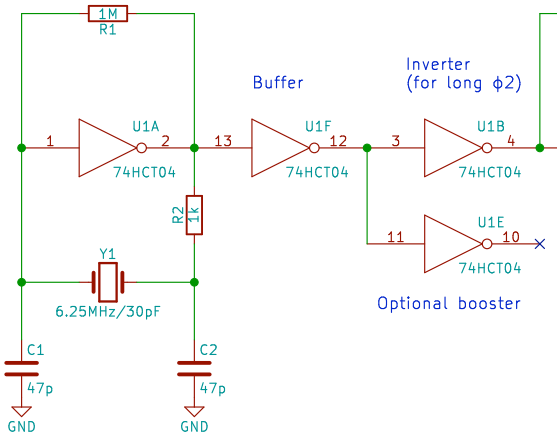
A decoupling (or bypass) capacitor in close proximity to every IC's power pin provides transient current when switching between logic levels.



Zener diode D1 protects the circuit against reverse current and overvoltage

Clock

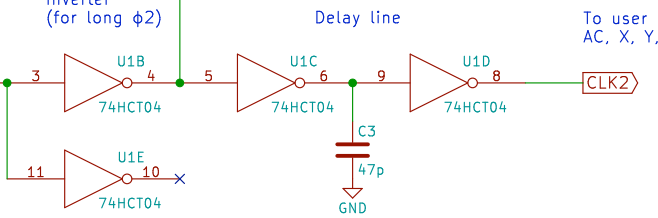
Pierce oscillator



Buffer

Inverter (for long ϕ2)

Delay line



Optional booster

To instruction fetch and control unit
PC, IR, D, WE

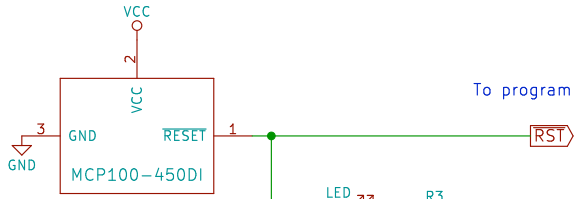
CLK1

To user registers
AC, X, Y, OUT

CLK2

The 47pF of C3 provides an additional CLK2−CLK1 shift of 5ns, which is required when using the original 70ns SRAM at 6.25MHz, or when overclocking in general. (It is not needed when using a 55ns SRAM module at 6.25MHz.)

Reset



To program counter PC

Power OK indicator

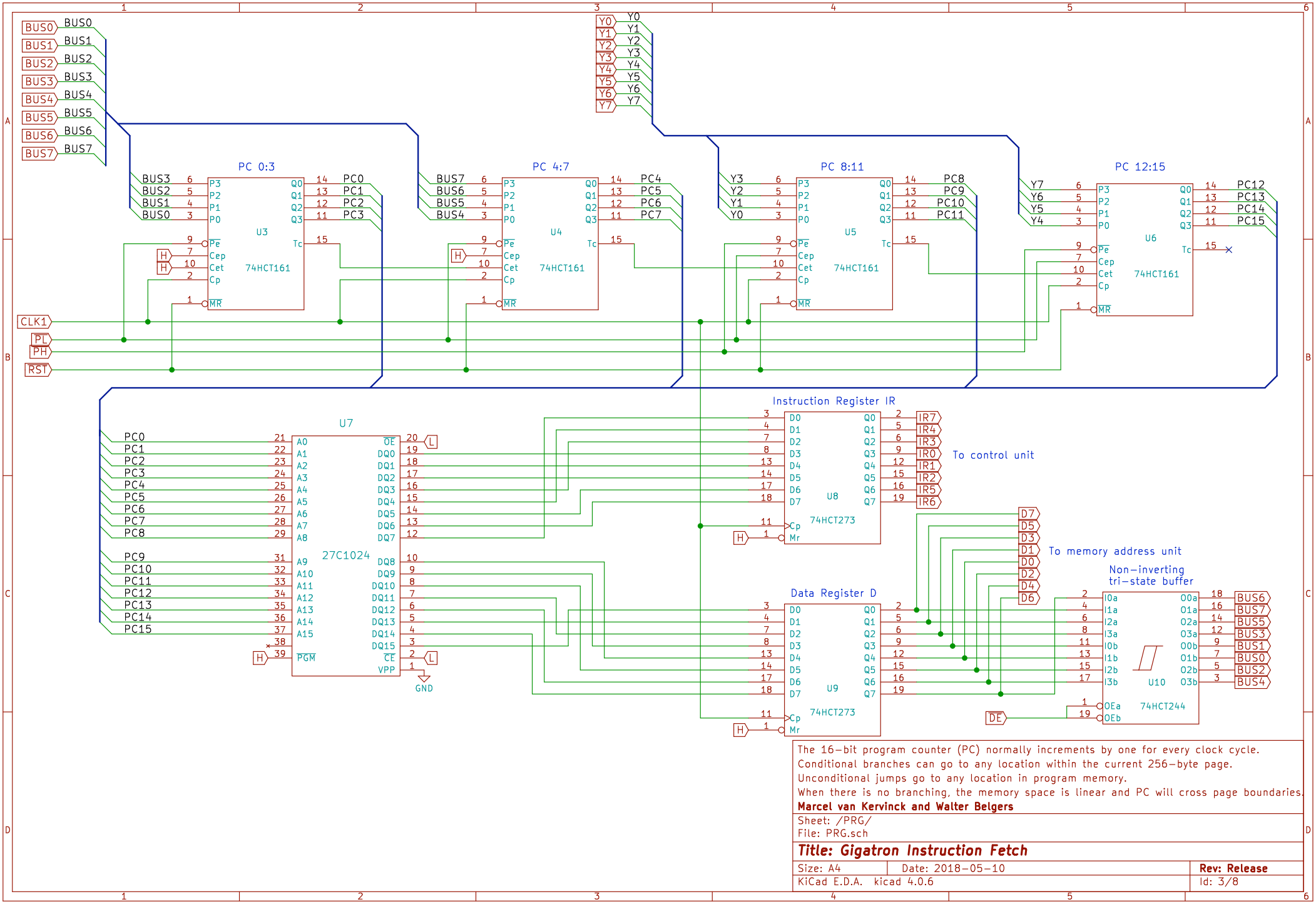
(1) Power comes from the +5V that a USB charger provides. The data lines are not used. (2) The oscillator generates 6.25MHz square waves. The HCT−inverter gives a long 2nd clock phase. This is useful for the /WE pulse derived from it. (3) The Power−On Reset (POR) supervisory circuit holds /RESET low for 350ms during power up and brown outs.

Marcel van Kervinck and Walter Belgers

Sheet: /PCR/
File: PCR.sch

Title: Gigatron Power, Clock and Reset

Size: A4	Date: 2018−05−10	**Rev: Release**
KiCad E.D.A. kicad 4.0.6		Id: 2/8



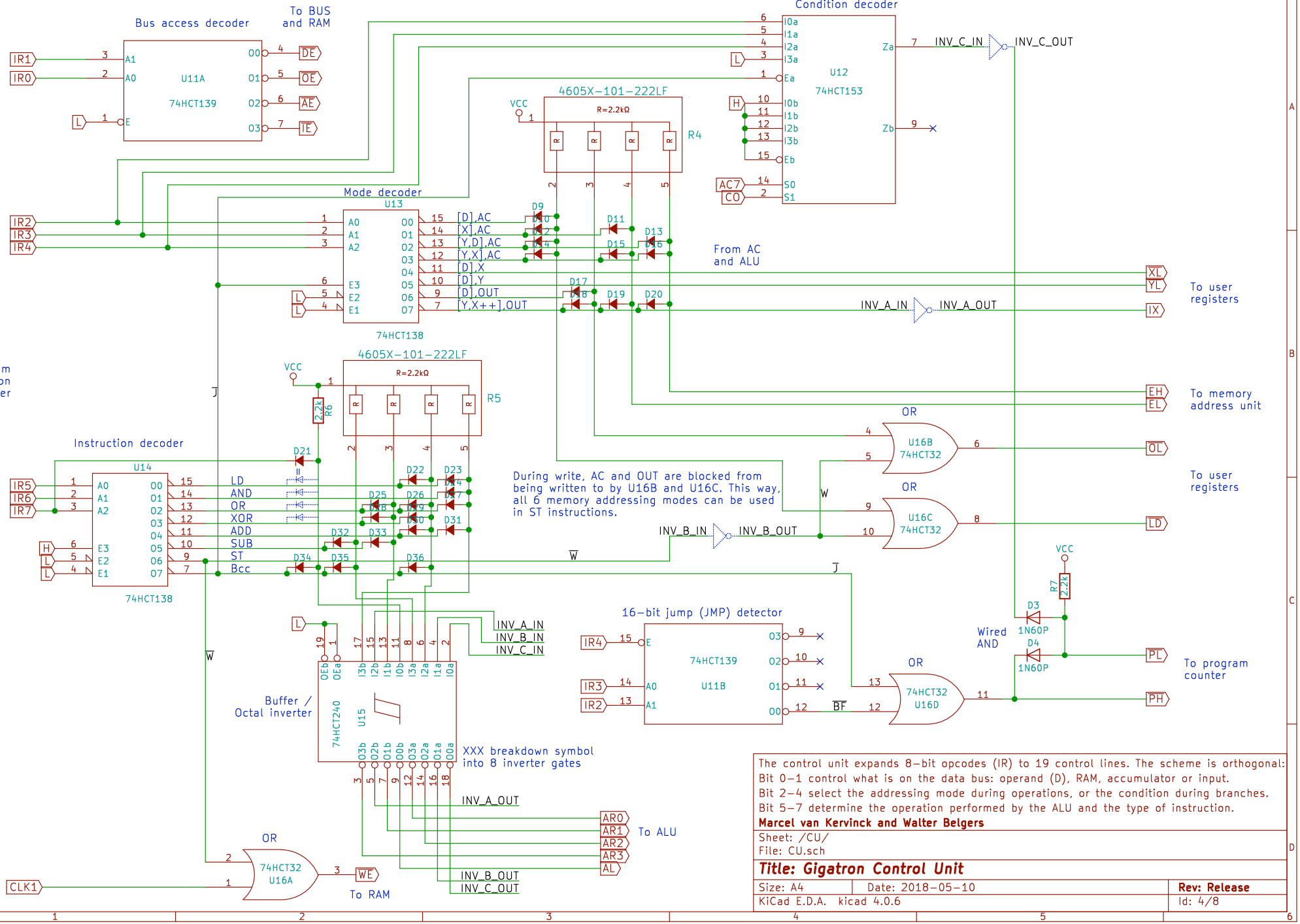
The 16−bit program counter (PC) normally increments by one for every clock cycle.
Conditional branches can go to any location within the current 256−byte page.
Unconditional jumps go to any location in program memory.
When there is no branching, the memory space is linear and PC will cross page boundaries.

Marcel van Kervinck and Walter Belgers

Sheet: /PRG/
File: PRG.sch

Title: Gigatron Instruction Fetch

Size: A4	Date: 2018−05−10	**Rev: Release**
KiCad E.D.A. kicad 4.0.6		Id: 3/8


Bus access decoder
To BUS and RAM
U11A
74HCT139
IR1
IR0
L
DE
OE
AE
TE
Condition decoder
U12
74HCT153
INV_C_IN
INV_C_OUT
4605X-101-222LF
R=2.2kΩ
R4
VCC
H
AC7
CO
Mode decoder
U13
74HCT138
IR2
IR3
IR4
[D],AC
[X],AC
[Y,D],AC
[Y,X],AC
[D],X
[D],Y
[D],OUT
[Y,X++],OUT
From AC and ALU
INV_A_IN
INV_A_OUT
XL
YL
IX
To user registers
From instruction register
J
4605X-101-222LF
R=2.2kΩ
R5
R6
2.2k
EH
EL
To memory address unit
Instruction decoder
U14
74HCT138
IR5
IR6
IR7
LD
AND
OR
XOR
ADD
SUB
ST
Bcc
OR
U16B
74HCT32
OL
During write, AC and OUT are blocked from being written to by U16B and U16C. This way, all 6 memory addressing modes can be used in ST instructions.
W
INV_B_IN
INV_B_OUT
U16C
74HCT32
LD
16-bit jump (JMP) detector
U11B
74HCT139
IR4
IR3
IR2
BF
U16D
74HCT32
Wired AND
D3
D4
1N60P
R7
2.2k
PL
PH
To program counter
Buffer / Octal inverter
U15
74HCT240
XXX breakdown symbol into 8 inverter gates
INV_A_IN
INV_B_IN
INV_C_IN
INV_A_OUT
INV_B_OUT
INV_C_OUT
AR0
AR1
AR2
AR3
AL
To ALU
CLK1
U16A
74HCT32
WE
To RAM
The control unit expands 8-bit opcodes (IR) to 19 control lines. The scheme is orthogonal:
Bit 0-1 control what is on the data bus: operand (D), RAM, accumulator or input.
Bit 2-4 select the addressing mode during operations, or the condition during branches.
Bit 5-7 determine the operation performed by the ALU and the type of instruction.
Marcel van Kervinck and Walter Belgers
Sheet: /CU/
File: CU.sch
Title: Gigatron Control Unit
Size: A4
Date: 2018-05-10
Rev: Release
KiCad E.D.A. kicad 4.0.6
Id: 4/8

Memory Address Unit

Quad 2:1 MUX

U35 74HCT157

X4 D4 X5 D5 X7 D7 X6 D6 L

I0a I1a I0b I1b I0c I1c I0d I1d S E

Za Zb Zc Zd

A4 A5 A7 A6

Quad 2:1 MUX

U34 74HCT157

X1 D1 X2 D2 X0 D0 X3 D3 EL L

A1 A2 A0 A3

Quad 2:1 MUX

U33 74HCT157

Y5 H Y6 H Y1 H Y3 H EH L

A13 A14 A9 A11

Quad 2:1 MUX

U32 74HCT157

Y0 H Y7 H Y4 H Y2 H L

A15 A15

A8 A12 A10

From control unit

32kB/70ns static RAM

U36 HM62256BLP-7

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14

D0 D1 D2 D3 D4 D5 D6 D7 BUS0 BUS1 BUS2 BUS3 BUS4 BUS5 BUS6 BUS7

OE WE CS OE WE L

The 6.25 MHz system has a clock period of 160 ns.
In each clock cycle 1 RAM access and 1 ALU operation can be done sequentually. Therefore the computer needs an SRAM speed of 70ns for reliable operation. In the kit 55ns SRAM is included for additional headroom.

EH	EL	AH	AL	Notation
L	L	YYYYYYYY	XXXXXXXX	[y,x]
L	H	YYYYYYYY	DDDDDDDD	[y,$dd]
H	L	00000000	XXXXXXXX	[x]
H	H	00000000	DDDDDDDD	[$dd]

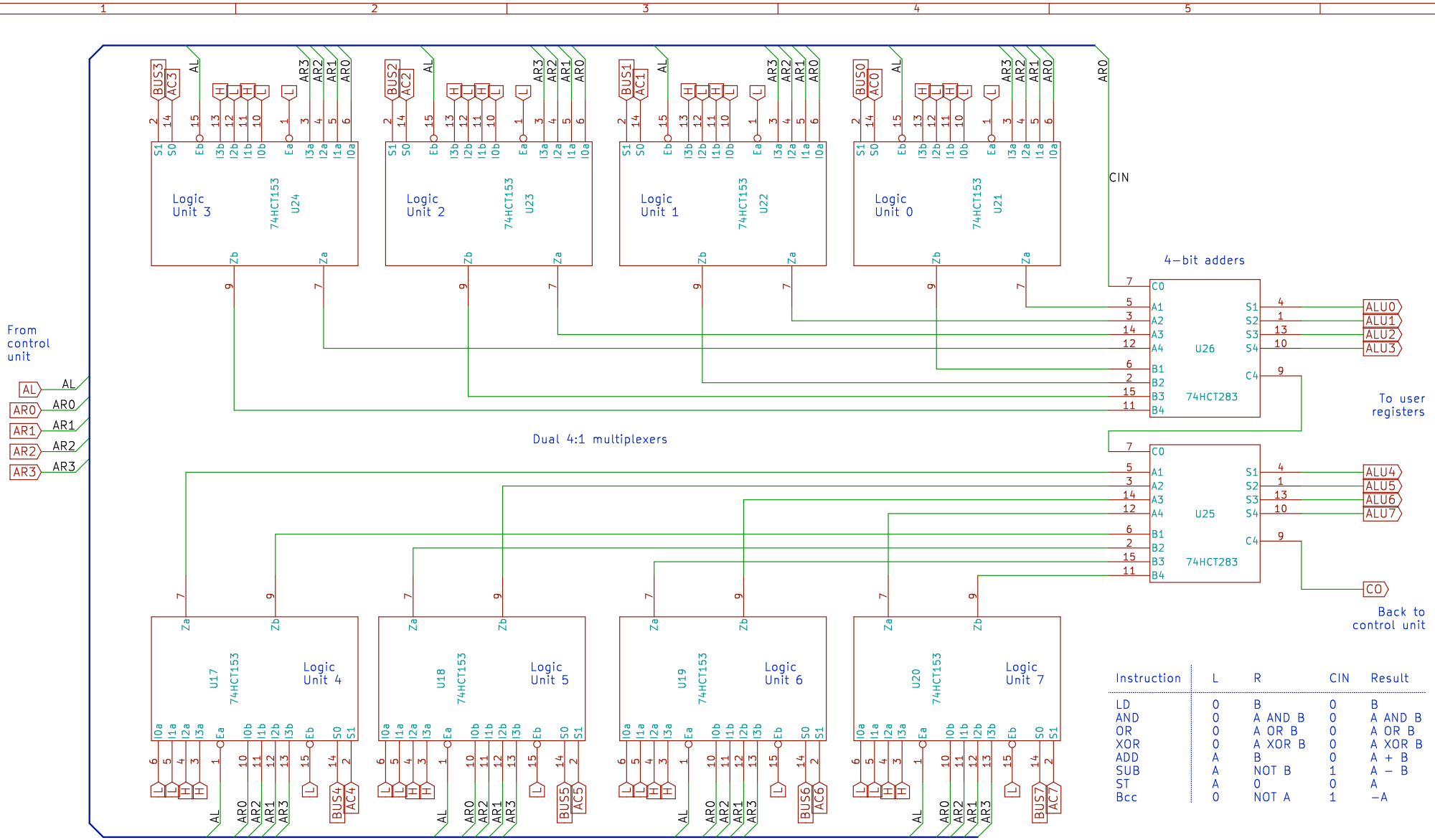
For speed and simplicity the memory addressing space is two-dimensional.
The address unit can create addresses in four different ways, as shown in the table.
The low address byte originates either from the operand (D) or from the user X register
The high address byte is either zero or comes from the user Y register.

Marcel van Kervinck and Walter Belgers

Sheet: /RAM/
File: RAM.sch

Title: Gigatron Memory and Address Unit

Size: A4	Date: 2018-05-10	**Rev: Release**
KiCad E.D.A. kicad 4.0.6		Id: 5/8



Instruction	L	R	CIN	Result
LD	0	B	0	B
AND	0	A AND B	0	A AND B
OR	0	A OR B	0	A OR B
XOR	0	A XOR B	0	A XOR B
ADD	A	B	0	A + B
SUB	A	NOT B	1	A − B
ST	A	0	0	A
Bcc	0	NOT A	1	−A

Each of the eight logic unit packages contains two 4:1 multiplexers we call L and R. R is fully programmable by the truth table hosted in the control unit (AR0:3). It performs logic functions on both accumulator (A) and bus data (B). L will either be zero or the value of the accumulator. Therefore it needs just one control line (AL).
The stage with two 4-bit adders combines L and R for a final result. The table lists resulting operations that we use.

During jump instructions, `-A' is computed so that the carry out (CO) indicates if the accumulator is zero.
During store instructions, `A' is `computed' so that, depending on addressing mode, the accumulator can be copied to X or Y as well.

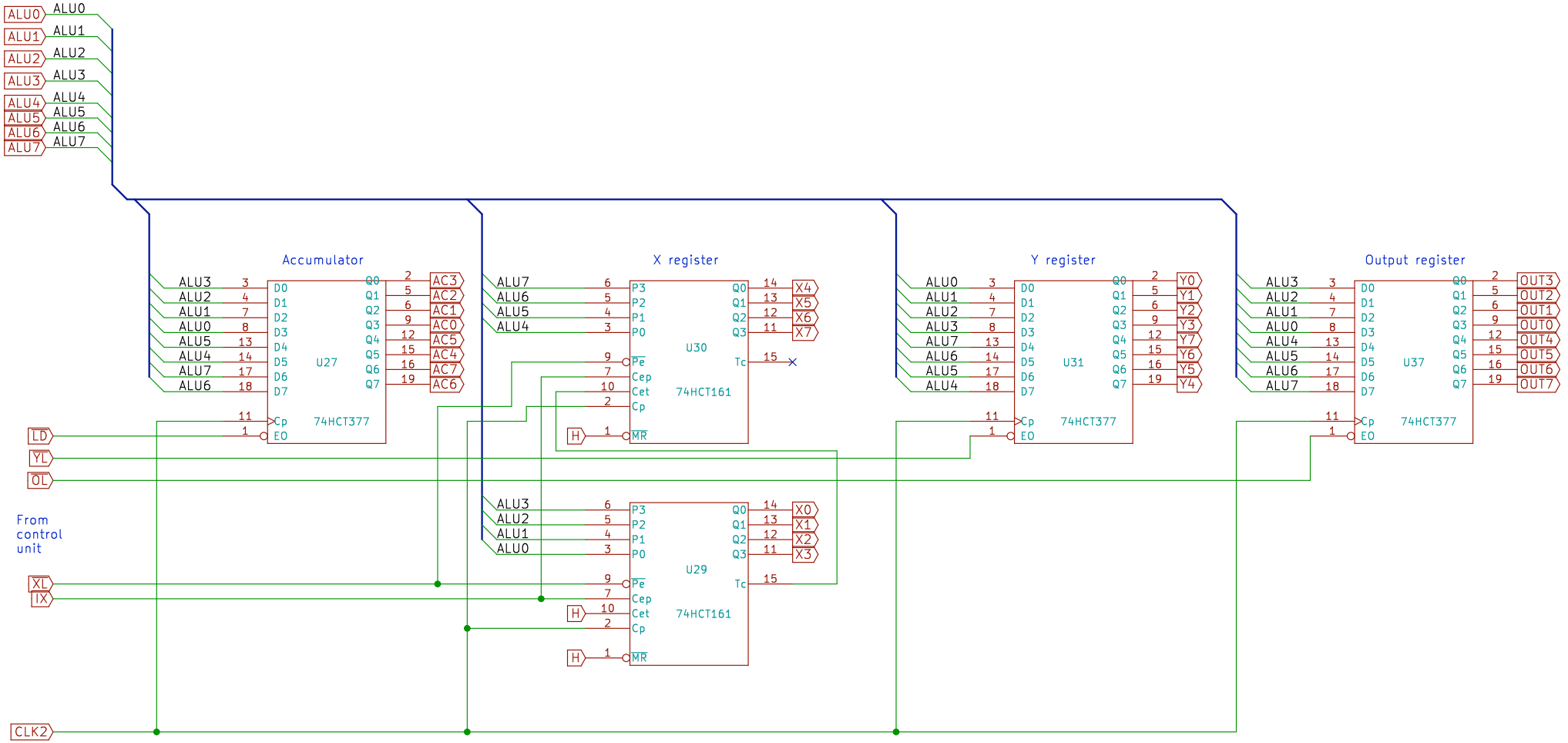
This unit is the equivalent of two large 4-bit 74181 ALU chips that were at the heart of many 1970s minicomputers. This design is inspired by Dieter Mueller's excellent notes starting from http://6502.org/users/dieter/a1/a1_4.htm

Marcel van Kervinck and Walter Belgers

Sheet: /ALU/
File: ALU.sch

Title: Gigatron Arithmetic and Logic Unit

Size: A4	Date: 2018-05-10	**Rev: Release**
KiCad E.D.A. kicad 4.0.6		Id: 6/8



Besides PC there are four user registers: AC, X, Y and OUT, each has 8-bits.
AC is the accumulator for calculations. X and Y are used to form memory addresses.
Y is also used by the JMP instruction. OUT is the primary output register.
Only AC can write back to memory, the others are effectively write-only.

Marcel van Kervinck and Walter Belgers

Sheet: /REG/
File: REG.sch

Title: Gigatron User Registers

Size: A4	Date: 2018-05-10	**Rev: Release**
KiCad E.D.A. kicad 4.0.6		Id: 7/8

The RGB resistor values depend on the 74xx sub-family of the OUT register:
7400/74LS: 390Ω / 820Ω
74HCT/HC: 750Ω / 1500Ω

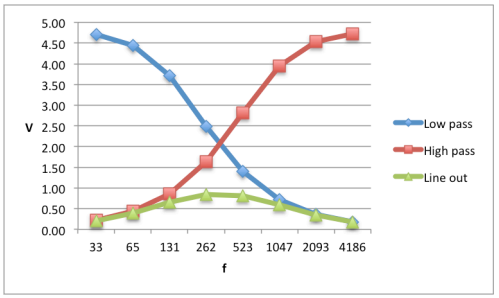
J3
DB15_FEMALE_HighDensity_MountingHoles

OUT0 1k5 R11 RED
OUT1 750 R12
OUT2 1k5 R13 GREEN
OUT3 750 R14
OUT4 1k5 R15 BLUE
OUT5 750 R16
OUT6 68 R17 HSYNC
OUT7 68 R18 VSYNC

GND

DB15 connector for 64 colors analog
RGB video out (VGA compatible)

Attenuation from 74HCT output to audio
line level by two overlapping filter slopes:
f_L (700Hz) > f_H (160Hz)



Blinkenlights

R8
R=2.2kΩ
LED D8
LED D7
LED D6
LED D5

Extended output

U38
74HCT273
AC3 AC2 AC1 AC0 AC4 AC5 AC6 AC7
D0 D1 D2 D3 D4 D5 D6 D7
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
Cp Mr
H

DAC
R=10kΩ
R9
OUT
Low pass
C43 0.1µ

AC coupling
High pass
C44 0.1µ
2.2k R10

Line out
J2
TIP TSH RSH RING SLEEVE
CONN-JACK-STEREO-R/A-3PIN-3.5MM

GND

Audio

3.5mm stereo audio connector
for PC speakers or amplifier

SER_PULSE
SER_LATCH
SER_DATA
VCC
2.2k R19

Game controller input

U39
74HC595
SER SRCLK SRCLR RCLK G
QA QB QC QD QE QF QG QH QH
BUS0 BUS1 BUS2 BUS3 BUS4 BUS5 BUS6 BUS7

J4
DB9_MALE_MountingHoles

DB9 connector for a
"Famiclone" game controller

OUT gives 6 color bits and 2 sync bits for VGA. XOUT is the extended output register.
XOUT is controlled indirectly through /HSYNC and AC. On a positive edge it clocks in AC.
XOUT drives 4 blinkenlights and simple 4-bits audio. The waveform comes from software.
/HSYNC and /VSYNC double as clocks for the game controller and receiving shift register.

Marcel van Kervinck and Walter Belgers

Sheet: /PER/
File: PER.sch

Title: Gigatron Peripherals

Size: A4	Date: 2018-05-10	**Rev: Release**
KiCad E.D.A. kicad 4.0.6		Id: 8/8